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09/824,890	04/02/2001	Kevin J McGrath	5500-54701	1609

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/824,890	Applicant(s) MCGRATH ET AL.	
	Examiner Aimee J Li	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2001 and 11 March 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2, 3, 4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 23 July 2001; CFR as received on 12 February 2002; IDS as received on 13 November 2002; and IDS as received on 11 March 2003.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Information Disclosure Statement

4. The IDS received on 15 November 2002 lists Richter et al., U.S. Patent Number 5,481,684 as a reference to be considered. This reference was already listed in the IDS received on 23 July 2001 and was not considered in the 15 November 2002 IDS since it was a duplicate listing.

Claim Objections

5. Claim 32 is objected to because of the following informalities: Please correct the phrase "said second operating mode being in said first state, and wherein said first operating mode" to read --said second operating mode *indication* being in said first state, and wherein said ~~first~~ *second* operating mode-- so that it is clear that the second prescribed condition being referred to is the one established in the first claim. The corrections have been highlighted in italics or

strikethrough. Appropriate correction is required. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-5, 14-20 and 22-23 are rejected under 35 U.S.C. 102(b) as being taught by James L. Turley's Advanced 80836 Programming Techniques (herein referred to as Turley).

8. Referring to claim 1, Turley has taught an apparatus comprising:

a. A first storage location configured to store a segment selector (Turley Page 47, Paragraph 3 and Page 63, Paragraph 4) identifying a segment descriptor (Turley Page 63, Paragraph 4) including a first operating mode indication and a second operating mode indication (Turley Page 49, Table: A segment descriptor; Pages 47-48, Paragraphs 5 to 2; Page 50, Figure 2-2; Page 51-52; Page 53, Paragraph 3; and Page 54, Table);

b. A second storage location configured to store an enable indication (Turley Page 26, Control Register 0, element PE), wherein said enable indication, said first operating mode indication, and said second operating mode indication are

indicative of an operating mode (Turley Page 48, Paragraph 3 and Page 178, Paragraphs 2-3); and

c. A processor configured to process an instruction according to said operating mode (Turley pages 45-52; 259-260; and 264-266).

9. Referring to claim 2, Turley has taught wherein said operating mode is a first operating mode if said enable indication is in an enabled state and said first operating mode indication is in a first state, and wherein said operating mode is a second operating mode if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state (Turley Page 51-52; Page 50, Figure 2-3; Pages 53-54, Paragraphs 3 to 1; and Page 55, Paragraph 1).

10. Referring to claim 3, Turley has taught wherein said second operating mode is one of a plurality of operating modes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication (Turley Page 51-52; Page 50, Figure 2-3; Pages 53-54, Paragraphs 3 to 1; and Page 55, Paragraph 1).

11. Referring to claims 4 and 5, Turley has taught wherein one of said plurality of operating modes is a 32 bit operating mode (Applicant Claim 4) and wherein one of said plurality of operating modes is a 16 bit operating mode (Applicant Claim 5) (Turley Page 53-54, Paragraphs 3 to 1).

12. Referring to claims 14-19, Turley has taught

a. Wherein said first storage location is a memory location (Applicant's claim 14) (Turley Page 47, Paragraph 3 and Page 63, Paragraph 4), general purpose register within said processor (Applicant's claim 15) (Turley Page 47, Paragraph 3 and Page 63, Paragraph 4), or a special purpose register within said processor (Applicant's claim 16) (Turley Page 47, Paragraph 3 and Page 63, Paragraph 4). In regards to Turley, the segment selector is stored in a register designed to hold the segment selector data, which means it is a type special purpose register. Also, a memory location, by definition, is a specified location within a computer storage device and a register is a computer storage device, which means that the register holding the segment selector is a type of memory location. A general purpose register, by definition, is a register that can be used for different purposes, including as a special handler of data, which means that a register which handles special data, such as a segment register, is a type of general purpose register. For more information regarding these definitions, please see Rosenberg's Dictionary of Computers, Information Processing, and Telecommunications 2nd Edition pages 256, 377, 526, and 592.

b. Wherein said second storage location is a memory location (Applicant's claim 17) (Turley Page 26, Control Register 0, element PE), general purpose register within said processor (Applicant's claim 18) (Turley Page 26, Control Register 0, element PE), or a special purpose register within said processor (Applicant's claim 18) (Turley Page 26, Control Register 0, element PE). In regards to Turley, the enable indication is stored in a register designed to hold the enable indication

data, which means it is a type special purpose register. Also, a memory location, by definition, is a specified location within a computer storage device and a register is a computer storage device, which means that the register holding the segment selector is a type of memory location. A general purpose register, by definition, is a register that can be used for different purposes, including as a special handler of data, which means that a register which handles special data, such as a segment register, is a type of general purpose register. For more information regarding these definitions, please see Rosenberg's Dictionary of Computers, Information Processing, and Telecommunications 2nd Edition pages 256, 377, 526, and 592.

13. Referring to claim 20, Turley has taught wherein said processor is configured to process said instruction by executing interpreter software which emulates said instruction (Turley pages 283-286).

14. Referring to claim 22, Turley has taught wherein, if said enable indication is in a disabled state, said first operating mode indication is undefined and said processor is configured to establish said operating mode responsive to said second operating mode indication (Turley Page 26, Control Register 0, element PE and Page 51-52).

15. Referring to claim 23, Turley has taught a method comprising:

a. Determining an operating mode in a processor (Turley Page 48, Paragraph 3 and Page 178, Paragraphs 2-3) in response an enable indication in a first storage location (Turley Page 176, Paragraph 1 and Page 178, Paragraph 2-3), a first operating mode indication in a segment descriptor, and a second operating mode

indication in said segment descriptor (Turley Page 49, Table: A segment descriptor; Pages 47-48, Paragraphs 5 to 2; Page 50, Figure 2-2; Page 51-52; Page 53, Paragraph 3; and Page 54, Table)

b. Fetching operands and generating addresses in response to said operating mode (Turley Page 52, Paragraph 2).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 6-7, 24-25, and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over James L. Turley's Advanced 80386 Programming Techniques (herein referred to as Turley) in view of Khalidi et al., U.S. Patent Number 5,479,627 (herein referred to as Khalidi).

18. Referring to claim 6, Turley has not explicitly taught wherein said first operating mode includes a default address size, which is greater than 32 bits. However, Turley has taught a first operating mode with a default address size, which is equal to 32, bits (Turley Pages 51-52 and Pages 53-54, Paragraphs 3 to 1). Khalidi has an address size, which is greater than 32 bits (Khalidi column 6, lines 25-57). A person of ordinary skill in the art at the time the invention was made would have recognized that the address size greater than 32 bits would allow for more address locations to be referenced. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the larger address size of Khalidi in the first operating mode of Turley to increase the addressable area of the device.

Also, the size of the address does not matter. See *In re Rose* 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

19. Referring to claim 7, Turley has taught wherein said first operating mode further includes a default operand size of 32 bits (Turley pages 259-260).

20. Referring to claim 24, Turley has taught wherein said determining comprises determining a first operating mode responsive to said enable indication is in an enabled state and said first operating mode indication is in a first state (Turley Page 51-52; Page 50, Figure 2-3; Pages 53-54, Paragraphs 3 to 1; and Page 55, Paragraph 1). Turley has not explicitly taught wherein said first operating mode includes a default address size greater than 32 bits. However, Turley has taught said operating mode includes a default address size (Turley Page 51, D Bit). Khalidi has taught virtual addresses are greater than 32 bits (Khalidi column 6, lines 25-27). A person of ordinary skill in the art at the time the invention was made would have recognized that the address size greater than 32 bits would allow for more address locations to be referenced. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the larger address size of Khalidi in the first operating mode of Turley to increase the addressable area of the device. Also, the size of the address does not matter. See *In re Rose* 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

21. Referring to claim 25, Turley has taught wherein said first operating mode includes a default operand size of 32 bits (Turley pages 259-260).

22. Referring to claim 32, Turley has taught wherein said determining further comprises determining a second operating mode responsive to said enable indication being in an enabled state, said first operating mode indication in said second state, and said second operating mode

indication being in said first state (Turley Page 51-52; Page 50, Figure 2-3; Pages 53-54, Paragraphs 3 to 1; and Page 55, Paragraph 1) and wherein said second operating mode includes a default address size of 32 bits (Turley Page 51, D Bit).

23. Referring to claim 33, Turley has taught wherein said determining further comprises determining one of a plurality of operating modes if said enable indication is in said enabled state and said first operating mode indication is in a second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication (Turley Page 51-52; Page 50, Figure 2-3; Pages 53-54, Paragraphs 3 to 1; and Page 55, Paragraph 1).

24. Claims 8-13 and 26-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over James L. Turley's Advanced 80386 Programming Techniques (herein referred to as Turley) in view of Schrofer, U.S. Patent Number 4,682,284 (herein referred to as Schrofer).

25. Referring to claims 8 and 26, Turley has taught

a. Wherein said segment descriptor is one of a plurality of segment descriptors stored in a descriptor table including a plurality of entries (Applicant's claim 8) (Turley page 59-61);

b. Wherein said segment descriptor is one of a plurality of segment descriptors stored in a descriptor table having a plurality of entries (Applicant's claim 26) (Turley page 59-61);

c. A second segment descriptor of said plurality of segment descriptors from said segment descriptor table (Applicant's claim 26) (Turley page 59-61).

26. Turley has not taught

a. Wherein at least one of said plurality of segment descriptors occupies two of said plurality of entries (Applicant's claim 8);

b. Wherein said second segment descriptor occupies up to two entries of said plurality of entries depending upon a type of said second segment descriptor (Applicant's claim 26).

27. Schrofer has taught

a. Wherein at least one of said plurality of segment descriptors occupies two of said plurality of entries (Applicant's claim 8) (Schrofer column 8, lines 27-42);

b. Wherein said second segment descriptor occupies up to two entries of said plurality of entries depending upon a type of said second segment descriptor (Applicant's claim 26) (Schrofer column 8, lines 27-42).

28. In regards to Schrofer, he has illustrated the use and need for the use of multiple storage locations for larger data words. A person of ordinary skill in the art at the time the invention was made would have recognized that multiple entries are needed to store larger data words, thereby increasing the accuracy and variety of data the system uses. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multiple storage locations of Schrofer in the device of Turley to increase the accuracy and variety of data used in the system.

29. Referring to claims 9 and 27, Turley has taught a call gate descriptor (Turley page 478).

30. Referring to claims 10 and 28, Turley has taught an interrupt gate descriptor (Turley 479).

31. Referring to claims 11 and 29, Turley has taught a trap gate descriptor (Turley page 479).

32. Referring to claims 12 and 30, Turley has taught a task state segment descriptor (Turley page 479).

33. Referring to claims 13 and 31, Turley has taught a local descriptor table descriptor (Turley page 480). In regards to Turley, an LDT is a local descriptor table.

34. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over James L. Turley's Advanced 80386 Programming Techniques (herein referred to as Turley) in view of Park, U.S. Patent Number 6,021,484 (herein referred to as Park). Turley has not taught wherein said processor is configured to process said instruction by executing translation software to translate said instruction into one or more native instructions to be executed by said processor. Park has taught wherein said processor is configured to process said instruction by executing translation software to translate said instruction into one or more native instructions to be executed by said processor (Park column 1, line 57 to column 2, line 8 and column 2, lines 48-59). In regards to Park, whether translating instructions is conducted in hardware or software, it does not matter since they are functionally equivalent. A person of ordinary skill in the art at the time the invention was made would have recognized that translation software increases compatibility between machines (Park column 1, lines 42-56).

Conclusion

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
June 1, 2004

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